

## 1 SYNCHRONIZED MULTI-OUTPUT DIGITAL CLOCK MANAGER

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8 ABSTRACT OF THE DISCLOSURE

9 A digital clock manager is provided. The digital clock  
10 manager generates an output clock signal that causes a  
11 skewed clock signal to be synchronized with a reference  
12 clock signal. Furthermore, the digital clock manager  
13 generates a frequency adjusted clock signal that is  
14 synchronized with the output clock signal during concurrence  
15 periods. The digital clock manager includes a delay lock  
16 loop and a digital frequency synthesizer. The delay lock  
17 loop generates a synchronizing clock signal that is provided  
18 to the digital frequency synthesizer. The output clock  
19 signal lags the synchronizing clock signal by a DLL output  
20 delay. Similarly, the frequency adjusted clock signal lags  
21 the synchronizing clock signal by a DFS output delay. By  
22 matching the DLL output delay to the DFS output delay, the  
23 digital clock manager synchronizes the output clock signal  
24 and the frequency adjusted clock signal.

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